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Original Research Article

Improving the Operating Speed of the Distance Protection Scheme of an 11 kV Distribution System using Microprocessors

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ABSTRACT

Distance relays and protection schemes are used in the protection of transmission and distribution lines. The speed of isolating faulty circuits from the network is relatively low and this operation speed was improved in this paper by using a microprocessor to make fast tripping decision for the relay. The microprocessor was programmed by using results obtained from fault studies carried out on the network. Using simulations in Power System Computer Aided Design (PSCAD) software, for a line-to-line (LLG) fault between lines A and B to ground (AB-G) occurring at 35 km on the tested line having a fault impedance of 5 Ω, the operating time of the developed system was 5.4 ms whereas it was 15 ms with the old system without the microprocessor (the conventional distance relay system). The new protection system working with the microprocessor was found to have improved the average operating speed of the distance protection scheme from 6.144 ms to 4.390 ms resulting to an improvement of the operating speed or speed of isolating faulty circuit by approximately 29%.

1. INTRODUCTION

Protection of the power systems (PS) and its equipment began with the use of fuses and manual circuit breakers at the end of the eighteenth century, (Obi et al. 2014; Obi et al. 2021). Thereafter, the use of relays to give automated protection to the system began with the over-current relays and under-voltage/over-voltage relays, (Goremykin 2023; Ahmed and El-Fergany, 2023; Kulikov et al. 2022; Nwachi et al. 2022). Finding the optimal values of time dial setting (TDS) and plug setting multiplier (PSM) of this can become a major challenge if not well coordinated. Thus, different algorithm/optimization techniques have been put forward to obtain optimal TDS and PSM of the relays. These include a new metaheuristic algorithm, the JAYA algorithm and the simplex method firefly algorithm (Pragati and Amol, 2017; Bedekar et al. 2010; Noghabi et al. 2009). More so, the fact that the operating time and pick up values of the overcurrent relays depend on the fault current which varies with the fault type and circuit characteristics, the overcurrent relay and protection scheme was less attractive in protecting high voltage systems (grids) where different power plants and load centers are interconnected. This is because any malfunction of this relay may cause instability in the concerned grid, (Fumilayo et al. 2012; Mahat et al. 2011; Keil and Jager, 2008). This challenge gave birth to the distance relay and protection scheme.

Though the distance relays have functioned effectively in protecting power systems, they has been characterized with some degree of inaccurate and relatively slow operations. Some of the causes of the comparatively low degree of accuracy and speed of operations in the distance relay include, (Ghorbani et al. 2021; Hosseinimoghadam et al. 2021; Ali et al. 2016; Mohajeri et al. 2015; Paithanar and Bhide, 2003):

(i) Variation of line parameters with atmospheric conditions and these line parameters are used in relay models.

(ii) DC offset values in fault current. Hence, the fault current which is the primary functional data of the relay carrying some form of 'impurity'.

(iii) Ambiguity about line parameters since the line parameters are seldom measured, they are calculated from the line data and again these line parameters are used in relay models.

It was also demonstrated that though the operational speed and accuracy of distance relays operations may be fair when the system experiences a single type of fault, the same cannot be said of the relays operations when the system experiences different types of fault simultaneously, (Abouelenin and Jabr 2002). In a review of recent techniques in protection of power lines, it was pointed out that the conventional distance relays are comparatively slow in their operations are less accurate in fault, location and isolations, (Babu et al. 2011; Zayandehroodi et al. 2015). It has also been found that the distance relay is characterized by indiscriminate tripping in the protection zones for different fault type and impedances (Onwuka et al. 2023).

Because of these and more, researchers have begun to move on from the distance relay to finding other improved device in protecting the power systems. A digital distance relay using field programmable gate arrays (FPGAs) technique for the detection of faults and possible isolation of the faulty circuit was developed by (Tsair-Fwu et al. 2006) and demonstrated that it has a relatively higher speed and accuracy than the conventional distance relays.

In recent times, the microprocessor relays are gradually taking the place of the conventional distance relays in protection systems especially in micro grid and low voltage networks (Akhmedova et al. 2021; Rajalwal and Ghosh, 2020; Bo et al. 2019; Rohadi, 2019). However, there are still a lot of existing power system networks that use the conventional distance relay – based protection scheme. This paper tends to improve the operating speed of theses distance relay protection scheme by incorporating a microprocessor to the relay operations. This will be done in such a way that the relay no longer takes current and voltage from the current transformer (CT) and voltage transformers (PT) but from the microprocessor, and the microprocessor will now be what takes signals from the CT/PT as shown in Figure 1.

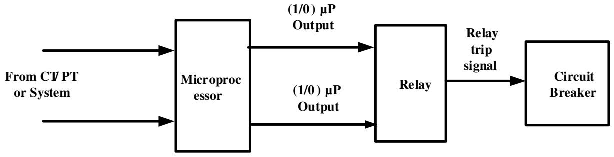


Figure 1: Block diagram for microprocessor – controlled relay protection philosophy

The current and voltage from the CT/PT are however rectified before been fed to the microprocessor. Also, since the microprocessor does not use current signal for its operations, a resistor is connected across the microprocessor so that the rectified current causes some voltage drop in the resistor connected across the microprocessor. It is this voltage drop signal in the resistor connected across that the microprocessor uses in place of the current signal. With this new system, the distance relay is relieved of the duty of impedance computation done by the relay before deciding whether to send trip signal to the circuit breaker (CB) or not. The microprocessor being very fast in computations and decision making processes is now deployed to do the computations and make decision whether to instruct the relay to send trip signal (a high (1) level signal) or restrain signal (low (0) level signal) to the relay. The distance relay now either send a trip or restrain signal to the CB after getting a 'I' or '0' signal from the microprocessor respectively.

The microprocessor works with a pre-defined program, the programming of the microprocessor is done with results from faults analysis of the system for different types of faults and faults impedances occurring at location on the line. The programming of the microprocessor is done by loading these results on the microprocessor and calling out the least fault current value from the results. The microprocessor then at any time compare the current and voltage from the CT/PT with the called-out least values from the fault analysis. If the current from the CT is at least equal to the least fault current recorded and the voltage from the PT is less than or equal to the least value from the fault analysis, then a high level ('1') (trip) signal is sent to the relay, else, a low level ('0') restrain signal is sent to the relay to perform no tripping action. The programming of the microprocessor is done using the 'C' programming language. This was tested using the Arduino simulator and it was found to output a high level signal when the conditions stated above were met.

However, the 'C' programming language is not compatible with the software used in this research (the PSCAD software), hence, an equivalent program of the 'C' programming language was developed in MATLAB (since MATLAB is compatible with PSCAD) and this was the code used for this work.

2. METHODOLOGY

2.1. Theoretical Analysis

The impedance seen by a distance relay for different types of fault in a line was modelled by (Onwuka et al, 2023) and is given as:

Impedance seen for a line to ground (L-G) fault is given by

$$Z_{seen}^{LG} = \frac{V_a}{I_a + K_0 I_a^0} = \frac{V_a^0 + V_a^1 + V_a^2}{I_a + K_0 I_a^0} \tag{1}$$

Where V_a=Phase voltage, I_a=Phase current.

Superscript 0, 1 and 2 are zero, positive and negative sequences, and K_0 is given as.

$$K_0 = \frac{Z_0 - Z_1}{Z_1} \tag{2}$$

For line to line (L-L) faults between 'a' and 'b', the potential between the lines is $V_a - V_b$ and the resultant current between the lines is $I_a - I_b$. The Impedance seen by the relay for this line to line (L-L) fault is given by;

$$Z_{seen}^{LL} = \frac{V_b - V_c}{I_b - I_c} = \frac{V_a^1 - V_a^2}{I_a^1 - I_a^2} \tag{3}$$

Also, the for a double line to ground (L-L-G) fault between lines 'b' and 'c' to ground,

$$V_b = V_a^0 + a^2 V_a^1 + a V_a^2 = V_c = V_a^0 + a V_a^1 + a^2 V_a^2 \tag{4}$$

And the fault current that flows in the lines 'b' and 'c' (combined) to ground is

$$I_b + I_c = I_a^0 + a^2 I_a^1 + a I_a^2 + I_a^0 + a I_a^1 + a^2 I_a^2 \tag{5}$$

since $1 + a + a^2 = 0$, rewrite Equation (5) as

$$I_b + I_c = 2I_a^0 - (I_a^1 + I_a^2) \tag{6}$$

Hence, the impedance seen by the relay is given as:

$$Z_{seen}^{LLG} = \frac{V_b(or\ V_c)}{I_b+I_c} = \frac{[V_a^0+a^2V_a^1+aV_a^2]or\ [V_a^0+aV_a^1+a^2V_a^2]}{2I_a^0-(I_a^1+I_a^2)} \tag{7}$$

Lastly. For faults involving all 3 phases, the impedance seen by the relay is simply

$$Z_{seen}^{3-\emptyset} = \frac{V_a}{I_a} = \frac{V_a^1}{I_a^1} \tag{8}$$

Taking the execution time of the above equation in PSCAD software will give us the speed of operation of this distance relay.

2.2. Test Network for the Study

To carry out this study, we shall use a 43km, 11kV power line running from Bus 1 to Bus 2 and protected by a 2 – zones, distance relay protection scheme as shown in Figure 2.

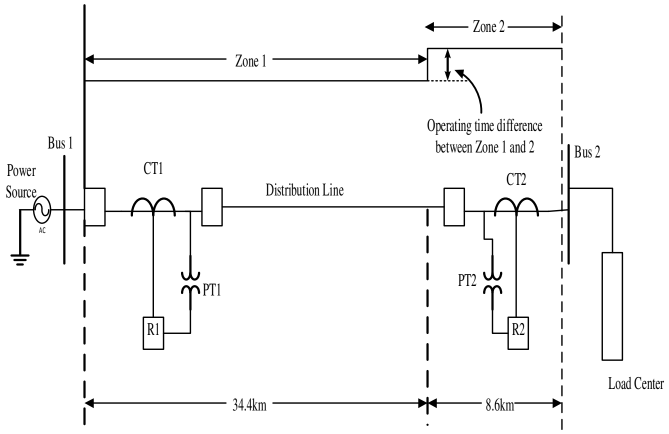


Figure 2: 2 – zone distance protection of an 11 kV power distribution line.

Zone 1 gives instantaneous protection to 80 % of the 43 km line (up to 34.4 km) while Zone 2 acts as a backup to Zone 1 for the first 80 % of the line and also protect the remaining 20% of the line (34.41 km to 43 km) and include some time delay. The line parameters of the line are presented in Table 1.

Table 1: Line parameters

Item/Description	Value
Length of line	43 km
Line Positive sequence resistance (same as negative sequence)	0.02582×10^{-3}(Ω/m)
Line Positive sequence reactance (same as negative sequence)	0.1291×10^{-3}(Ω/m)
Line Positive sequence capacitance (same as negative sequence)	$210.10(\Omega/\Omega^{-1})$
Line Zero sequence resistance	0.1365×10^{-3}(Ω/m)
Line Zero sequence reactance	1.021×10^{-3}(Ω/m)
Line Zero sequence capacitance	$423.251710(\Omega/\Omega^{-1})$
Fault impedance used	Fault ON resistance 10Ω Fault OFF resistance 1.0E6 Ω
K	6.826∠4.23°
Zone 1 (One)	0.0 km to 34.4 km
Zone 2 (Two)	34.41 km to 43 km

2.3. PSCAD Model for the Test Network

The modelling of the conventional relay operations in PSCAD is as shown in the block diagram of Figure 3 (Oputa et al, 2023). However, for the developed/improved protection system where the operations of the relay is controlled by the microprocessor, the model of the protection system in PSCAD is as shown in Figure 4. Note that in this particular model, the sequence components are not used. The current flowing in the line and the bus voltages (fault current and voltage at fault) are compared to the minimum value (reference voltage and current) got from all the results of the fault analysis conducted to determine whether a high or low signal will be sent by the microprocessor to the relay.

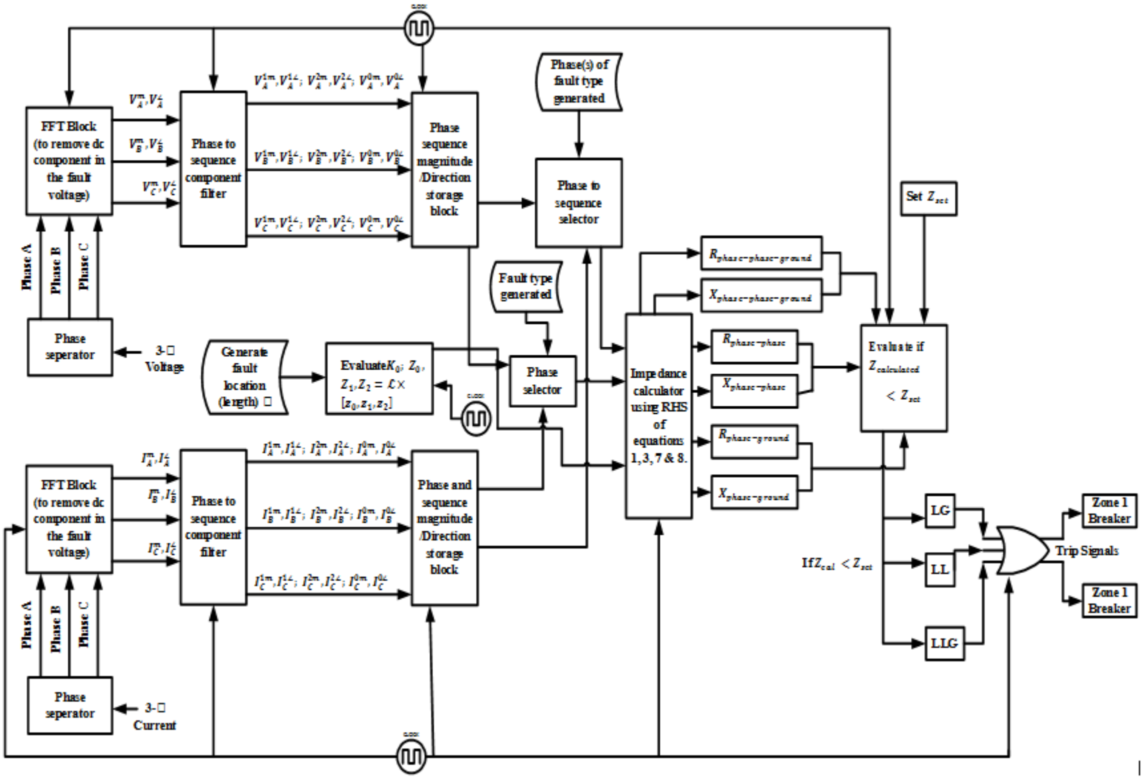


Figure 3: Block diagram of distance relay model in PSCAD.

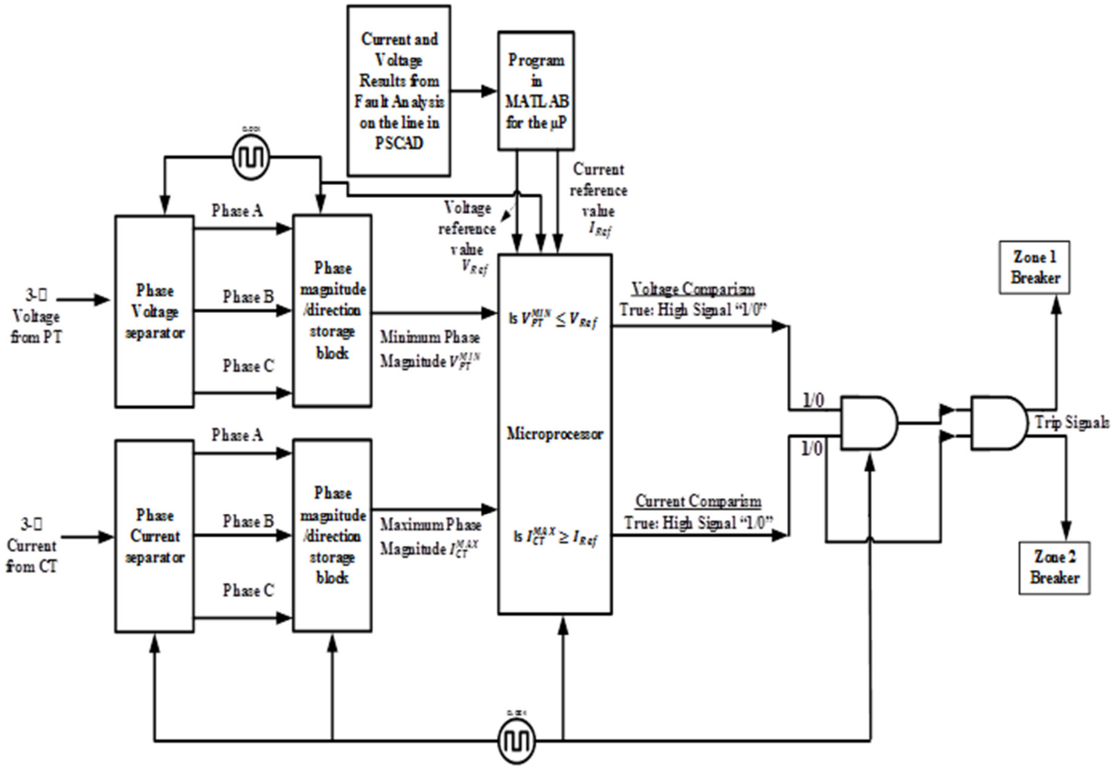


Figure 4: Block diagram of microprocessor controlled – relay model in PSCAD

3. RESULTS AND DISCUSSION

3.1. Results of Fault Analysis of the Network

The fault analysis of the system is done using the multi-run application in PSCAD for selected fault impedance of 0.1 Ω, 0.5 Ω, 1 Ω, 5 Ω, and 10 Ω for 10 (ten) types of fault (AG, BG, CG, AB, AC, BC, ABG, ACG, BCG and ABC faults). The locations of these faults were simulated at 50 m (from the sending end which is bus 1), 8.6 km, 17.2 km, 25.6 km, 34.4 km, 35 km, and 42.7 km along the line. A total of 350 set of results were recorded; there are 250 results (run numbers) for the faults in Zone 1 and 100 results for Zone 2. Some of the results recorded are presented in Tables 2 and 3.

3.2. Protection of the System

We shall in this section consider and compare how the conventional distance relay protection scheme and the developed microprocessor – controlled relay protection systems protect the test system for different types of fault, different fault impedance and fault locations. Considering a 10 Ω LG fault between line A and ground (AG) occurring at Zone 1 (10 km) on the line (from bus 1), the trip signal to the breaker was sent after 13 ms and 3.5 ms for the conventional distance relay protection scheme and the developed respectively and it is shown in the simulation result shown in Figures 5a and 5b. The fault is always introduced 1 s from the simulation. The operating time of the relay is the time the trip signal is sent after the introduction of the fault. Also, for a LLG fault (AB-G) of 10 Ω simulated at a location of 10 km on the line, the protection result from the conventional and developed system are as shown in Figure 6a and 6b respectively with a trip time of 15 ms and 3.5 ms. For faults simulated at a location of 35 km on the line, the protection speed is as shown in Figures 7a, 7b, 8a and 8b. The results show that for a 10 Ω LL (AB) fault, the trip time are 14.3 ms and 5.6 ms for the conventional relay and the developed system respectively. Also, for a 3 – Phase fault, the trip time are 14.3 ms and 5.6 ms for the conventional relay and the developed system respectively. Table 4 gives a comparison between the conventional relay system and the developed microprocessor – controlled protection system.

Table 2: Result of fault analysis of Zone 1 on the line

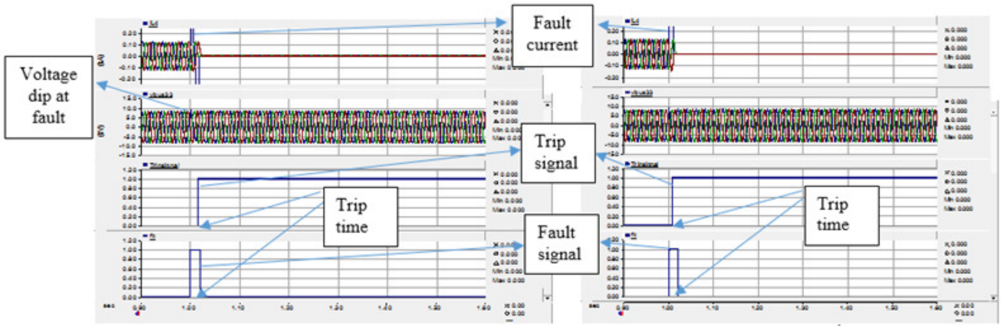
Run No	Fault location	Fault type	Fault resistance (Ω)	Fault current (kA)	Fault voltage (kV)
1	1	1	0.1000	0.8700970536	8.557641501
2	1	2	0.5000	0.8717600604	8.739286191
3	5	4	1.0000	0.2668940697	8.498807227
4	3	7	5.0000	0.4188353484	8.594634490

Key to Table 2: Fault Locations: 1 = 50 m on the line; 3 = 17.2 Km on the line; 5 = 34.4 Km on the line.
Fault Types: 1 = A-G Fault; 2 = B-G Fault; 4 = AB-G Fault; 7 = BC Fault; (Among others)

Table 3: Result of fault analysis of Zone 2 on the line

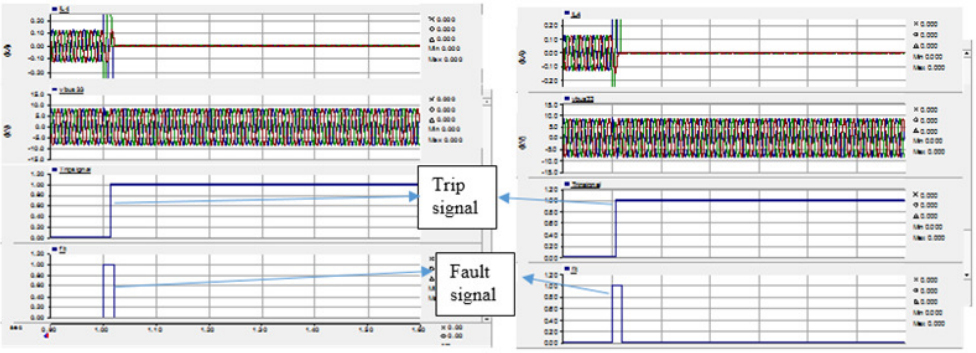
Run No	Fault location	Fault type	Fault resistance (Ω)	Fault current (kA)	Fault voltage (kV)
1	1	1	0.1000	0.3422416257	8.557953815
2	2	2	0.5000	0.2988388919	8.327978741
3	1	4	1.0000	0.4167304882	8.594886558
4	2	3	5.0000	0.3253819598	8.327978741
5	1	5	10.0000	0.4393926997	8.586453564

Key to Table 3: Fault Locations: 1 = 35 km on the line; 2 = 42.7 Km on the line
Fault Types: 5 = AC-G Fault; 9 = AC Fault; 3 = C-G Fault; 7 = ABC Fault; (Among others)



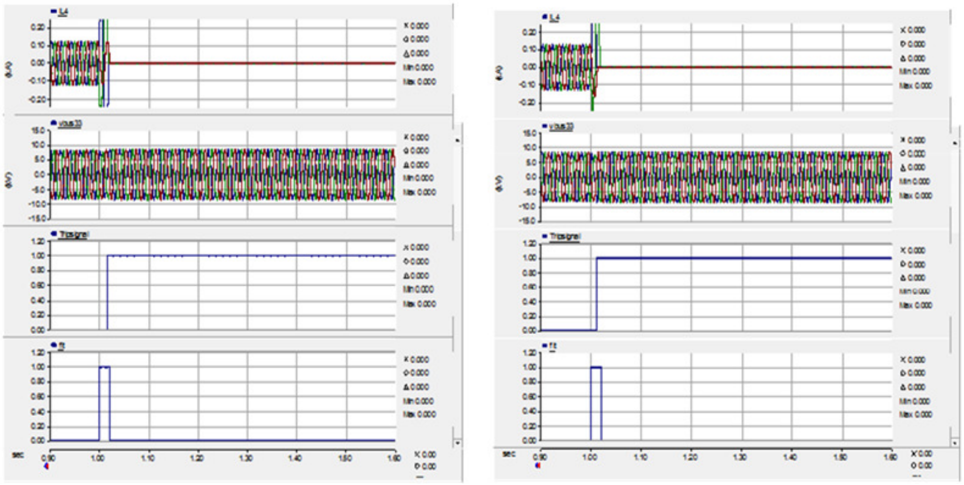
(a) (b)

Figure 5: 10Ω LG fault at 10 km for (a) conventional scheme and (b) developed system



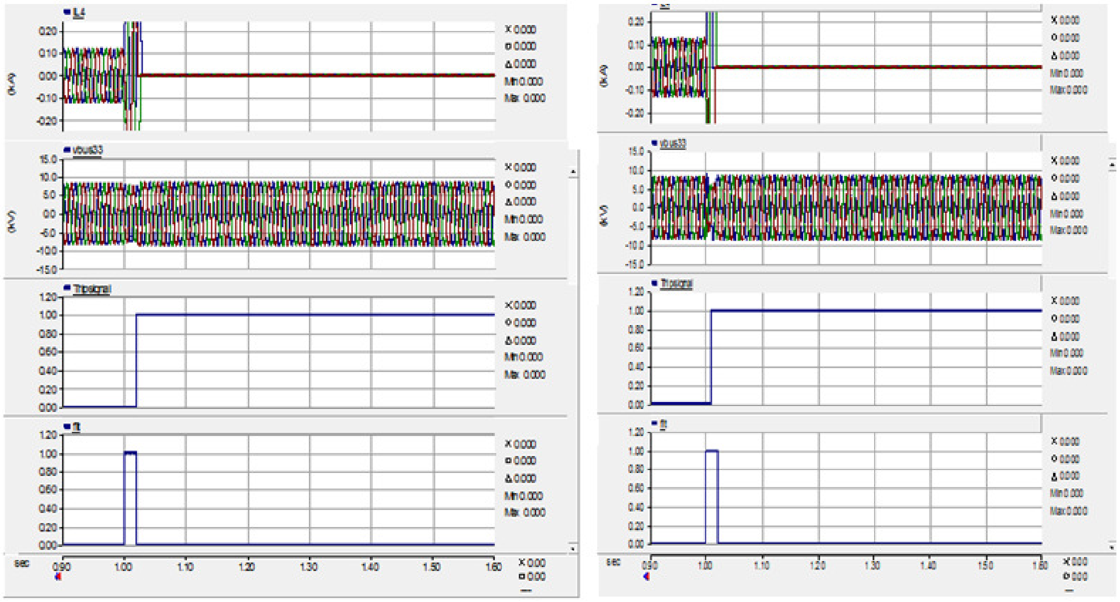
(a) (b)

Figure 6: 10Ω LLG fault at 10 km for (a) conventional scheme and (b) developed system



(a) (b)

Figure 7: 10Ω LG fault at 35 km for (a) conventional scheme and (b) developed system



(a) (b)

Figure 8: 10Ω 3 phase fault at 35 km for (a) conventional scheme and (b) developed system

Table 4: Comparison of the conventional distance relay and the developed system tripping time for different fault type, impedance and fault locations

Fault Location (km)	Fault Impedance (Ω)	Fault type	Trip time (ms) for conventional relay	Trip time (ms) for developed system	Trip time Difference. (ms
10.00	0.1	LG (AG)	5.00	3.3	1.7
		LL (AB)	7.50	3.3	4.2
		LLG (ABG)	6.25	3.3	2.95
		3 Phase	6.25	3.3	2.95
10.00	0.5	LG (AG)	6.25	3.4	2.85
		LL (AB)	6.25	3.3	2.95
		LLG (ABG)	6.25	3.4	2.85
		3 Phase	6.25	3.3	2.95
10.00	1.0	LG (AG)	6.25	3.5	2.75
		LL (AB)	7.50	3.4	4.1
		LLG (ABG)	7.00	3.5	3.5
		3 Phase	6.25	3.5	2.75
10.00	5.0	LG (AG)	6.25	3.4	2.85
		LL (AB)	11.25	3.4	7.85
		LLG (ABG)	6.25	3.5	2.75
		3 Phase	7.50	3.5	4.00
10.00	10.0	LG (AG)	13.00	3.5	9.25
		LL (AB)	11.00	3.6	7.40
		LLG (ABG)	12.00	3.5	8.50
		3 Phase	15.00	3.5	11.25
35.00	0.1	LG (AG)	8.75	5.2	3.55
		LL (AB)	13.75	5.1	8.65
		LLG (ABG)	7.50	5.2	2.30
		3 Phase	8.75	5.2	3.55
35.00	0.5	LG (AG)	8.75	5.2	3.55
		LL (AB)	15.00	5.3	9.7
		LLG (ABG)	8.75	5.3	3.45
		3 Phase	8.75	5.2	3.55
35.00	1.0	LG (AG)	10.00	5.4	4.6
		LL (AB)	13.75	5.4	8.35
		LLG (ABG)	10.00	5.4	4.6
		3 Phase	8.75	5.3	3.45
35.00	5.0	LG (AG)	15.00	5.4	9.6
		LL (AB)	13.75	5.5	8.25
		LLG (ABG)	15.00	5.4	9.6
		3 Phase	15.00	5.4	9.6
35.00	10.0	LG (AG)	17.50	5.6	11.9
		LL (AB)	14.30	5.6	8.7
		LLG (ABG)	18.80	5.6	13.20
		3 Phase	20.00	5.5	14.5

The average operating speed (AOS) of each protection scheme can be calculated as;

$$AOS = \frac{\sum_{i=1}^{40} Triptime_i}{40} \tag{9}$$

Where $Triptime_i$ is the time of operation of the protection scheme for the i^{th} protection study case (a total of 40 protection study cases in all for the conventional and designed protection schemes).

For the conventional distance relay protection scheme,

$$AOS_{CRS} = \frac{\sum_{i=1}^{40} Triptime_i}{40} = \frac{245.75}{40} = 6.144ms$$

AOS_{CRS} is average operating speed of the conventional distance relay protection scheme, while for the developed protection scheme,

$$AOS_{\mu PS} = \frac{\sum_{i=1}^{40} Triptime_i}{40} = \frac{175.6}{40} = 4.390ms$$

$AOS_{\mu PS}$ is average operating speed for the developed system with microprocessor.

It could be seen that for a particular fault type, fault impedance value and location of fault, the developed protection system operating time or trip time is comparatively lower than the conventional distance relay protection scheme. For example, for a 1.0 Ω LG fault simulated at 10 km on the line, the conventional distance relay sent trip signal to the CB to trip after 6.25 ms; however, the trip signal was sent to the CB after 3.5 ms for the developed protection system where the microprocessor controls the relay operations. Also, for a 0.5 Ω LLG fault simulated at 35 km on the line, the conventional distance relay sent trip signal to the CB to trip after 8.75 ms; however, the trip signal was sent to the CB after 5.3 ms for the developed protection system where the microprocessor controls the relay operation.

4. CONCLUSION

The operating speed of the distance relay was improved from an average of 6.144 ms to an average of 4.390 ms by controlling the relay by a microprocessor as demonstrated. This represents an approximate 28.5 % operating speed improvement of the existing distance relay protection scheme.

5. CONFLICT OF INTEREST

There is no conflict of interest associated with this work.

REFERENCES

Abouelenin, F. M. and Jabr, H. M. (2002). Behavior study of polarized distance relay in presence of the simultaneous faults. *11th IEEE Mediterranean Electro technical Conference (IEEE Cat. No.02CH37379), Cairo, Egypt*, pp. 517 – 521.

Ahmed, M. A. and El-Fergany, A. A. (2023). Protective Relaying Coordination in Power Systems Comprising Renewable Sources: Challenges and Future Insights" *Sustainability*, 15(9), pp. 154 – 167.

Akhmedova, O., Soshinov, A., Gazizov, F. and Ilyashenko, S. (2020). Development of an Intelligent System for Distance Relay Protection with Adaptive Algorithms for Determining the Operation Set Points. *Energies*, 14(4), pp. 173 – 188.

Ali, S. M., Abdel-Aziz, A. M., and Refai, R. A. (2016). Comparative Study between different methods used in protection by Distance of electrical Networks. *Journal of Al Azhar University Engineering Sector.* 11(3), pp. 557-570.

Babu, K. V., Tripathy, M and Singh, A. K. (2011). Recent techniques used in transmission line protection: a review. *International Journal of Engineering, Science and Technology*. 3(3), pp. 1 – 8.

Bedekar, P. P., Bhide, S. R. and Kale, V. S. (2010). Optimum Coordination of Overcurrent Relay Timing Using Simplex Method. *Electric Power Components and Systems, 38*, pp. 1175 – 1193.

Bo, Z. Q., Lin, X. N., Wang, Q. P., Yi, Y. H. and Zhou, F. Q. (2016) . Developments of power system protection and control. *Protection and Control of Modern Power Systems,* 3(4), pp. 28 – 36.

Funmilayo, H. B., Silva, J. A. and Butler-Purry, K. L. (2012). Overcurrent Protection for the IEEE 34-Node Radial Test Feeder. *IEEE Trans. Power Del.,* 27(2), pp. 459 – 468.

Ghorbani, A., Sanaye-Pasand, M. and Mehrjerdi, H. (2021). Accelerated distance protection for transmission lines based on accurate fault location" *Electric Power Systems Research*, 193, pp. 273 – 285.

Goremykin, S. A. (2023). Relay protection and automation of electric power systems. *Moscow: INFRA-M.* DOI: 10.12737/1048841 Retrieved from https://naukaru.ru/en/nauka/textbook/3202/view (Date of access 25.07.2023)

Hosseinimoghadam, S. M. S., Dashtdar, M., and Majid, D. (2021). Improving the performance of distance relays in the protection of short transmission lines based on the current estimation of the line end. *U. P. B. Sci Bull. Series C*, 83(1), pp. 752 – 781.

Keil, T and Jager, J. (2008). Advanced Coordination Method for Overcurrent Protection Relays Using Nonstandard Tripping Characteristics. *IEEE Trans. Power Del.*, 23(1), pp. 52-57.

Kulikov, A., Loskutov, A. and Bezdushniy, D. (2022). Relay Protection and Automation Algorithms of Electrical Networks Based on Simulation and Machine Learning Methods. *Energies,* 15(18), pp. 652 – 659.

Noghabi, A. S., Sadeh, J. and Mashhadi, H. R. (2009). Considering Different Network Topologies in Optimal Overcurrent Relay Coordination Using a Hybrid GA. *IEEE Transactions on Power Delivery*, 24(4), pp. 1857 – 1863.

Mahat, P., Chen, Z., Jensen, B. B. and Bak, C. L. (2011). A Simple Adaptive Overcurrent Protection of Distribution Systems with Distributed Generation. *IEEE Trans. Smart Grid,* 2(3), pp. 428 – 437.

Mohajeri, A., Seyedi, H., and Sabahi, M. (2015). Optimal Setting of Distance relays quadrilateral characteristic considering the uncertain effective parameters. *International Journal of Electrical Power and Energy Systems*. 73(1), pp. 1051-1059.

Nwachi, G. U., Obi, P. I., Amako, E. A. and Ezeonye, C. S. (2022). Modeling and Simulation of a Coordinated Power System Protection using Overcurrent Relay," *Nigerian Research Journal of Engineering and Environmental Sciences,* 7(1), pp. 238 – 249.

Obi, P. I., Chidolue, G. C. and Okonkwo, I. I. (2014). Protection and Control of Power Systems – A Review. *International Journal of Advancements in Research and Technology (IJOART),* 2(5), pp. 421 – 427.

Obi, P. I., Ezeonye, C. S., and Amako, E. A. (2021). Application of various Types of Circuit breakers in power systems: A Review. *Arid Zone Journal of Engineering, Technology and Environment.* 17(4), pp. 481 – 494.

Onwuka, I. K., Oputa, O., Diyoke, G. C., Ezeonye, C. S. and Obi, P. I. (2023). Effects of Varying Fault Impedance on Distance Protection Scheme of 11kV Distribution Systems. *Beyero Journal of Engineering and Technology (BJET),* 18(2), pp. 84 – 94.

Oputa, O., Ogbuka, C.U., Diyoke, G.C., Onwuka, I.K. and Madueme, T.C. (2023). Tripping Zone Accuracy of Distance Relay Protection for a 33kV Distribution System with Varying Fault Type and Impedance. *Nigerian Research Journal of Engineering and Environmental Sciences*, 8(2), pp. 586 – 595.

Paithanar, Y. G. and Bhide, S. R. (2003). Fundamental of powers system protection. *Prentice Hall of India private limited.*

Pragati, B. A. and Amol, K. A. (2017). Optimum Coordination of Overcurrent and Distance Relays Using JAYA Optimization Algorithm. *2017 International Conference on Nascent Technologies in the Engineering Field, Navi Mumbai*, *India,* pp.1 – 5.

Rajalwal, N. K. and Ghosh, D. (2020). Recent trends in integrity protection of power system: A literature review. *International Transactions on Electrical Energy Systems*, 30(2), pp. 253 – 262. https://doi.org/10.1002/2050-7038.12523.

Rohadi, N. (2005). Parametric sensitivity analysis of SEL-421 distance relay algorithms used in compensated line. *IOP Conf. Ser.: Mater. Sci. Eng.* pp. 1 – 9.

Tsair-Fwu, L., Cho, M., Ying-Chang, H. and Hong-Jen, L. (2006). An Embedded Methodology for FPGAs' Digital Distance Relay Design and Analysis. *2006 International Conference on Hybrid Information Technology,* pp. 33 – 41.

Zayandehroodi, H., Gorooh, A. A. and Azimizadeh, H. (2015). Structure and Technology of the Numerical Relay Protection in the Power Systems. *Cumhuriyet University Faculty of Science Journal (CSJ)*, 36(6), pp. 1 – 7.